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United States Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW	Docket Number (Optional) 058268.00327
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on _____ Signature _____ Typed or printed Name _____	Application Number: 10/750,961 Filed: January 5, 2004 First Named Inventor: Jiann-Jyh (James) LAY Art Unit: 2113 Examiner: Y.L. WILSON

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

Arlene P. Neal
Signature

☐ Applicant/Inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed

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Reg. No. is acting under 37 CFR 1.34 _____

January 22, 2008
Date

NOTE: Signatures of all of the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Jiann-Jyh (James) LAY

Serial No.: 10/750,961 Group Art Unit: 2113

Filed: January 5, 2004 Atty. Docket No.: 058268.00327

For: SYSTEM AND METHOD FOR SELF-ADAPATIVE REDUNDANCY CHOICE LOGIC

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450 **January 22, 2008**

Sir:

In accordance with the Pre-Appeal Brief Conference Pilot Program guidelines set forth in the July 12, 2005 Official Gazette Notice, Applicant hereby submits this Pre-Appeal Brief Request for Review of the final rejections of claims 1-6, 8-16, 18 and 19 in the above identified application. Claims 1-6, 8-16, 18 and 19 were finally rejected in the Office Action dated September 19, 2007. Applicant filed a Response to the Final Office Action on December 7, 2007, and the Office issued an Advisory Action dated December 19, 2007 maintaining the final rejections of claims 1-6, 8-16, 18 and 19. Applicant hereby appeals these rejections and submit this Pre-Appeal Brief Request for Review. This Pre-Appeal Brief Request for Review is being timely filed. As will be discussed below, numerous clear errors exist in the final rejections that require withdrawal thereof.

Claims 1-6, 10, 11, and 14-16 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,728,910 to Huang (hereinafter Huang '910). As outlined below, Huang '910 fails to disclose or suggest each of elements of claims 1-6, 10, 11, and 14-16. The failure of Huang '910 to disclose each and every element of the present claims constitutes clear error.

Huang '910 teaches a method for self-test and self-repair of a semiconductor memory device. A single built-in self-test (BIST) engine with an extended address range is used to test the entirety of memory, i.e., both redundant and accessible memory portions, as a single array, preferably using a checkerboard bit pattern. In a first stage, faulty rows in each memory portion are identified and their addresses recorded. Known-bad rows in accessible memory are then replaced by known-good redundant rows, and the resulting repaired memory is retested in a second stage. During a second stage, repair of the accessible memory portion is verified, while defects among the redundant portion are ignored.

Applicant submits that the rejection of claims 1-6, 10, 11, and 14-16 under 35 U.S.C. 102(e) based on the teachings of Huang '910 is clearly erroneous. Applicant submits that Huang '910 does not teach or suggest each element of the presently pending claims. Each of the presently pending claims recites, in part, repeating selection of an alternate redundant memory section, if the selected redundant memory section or the selected alternated redundant memory section is non-functional, until at least one of the selected redundant memory section or the selected alternated redundant memory section is determined to be functional or all redundant memory sections have been selected. Huang '910 does not teach or suggest at least these features.

Rather, Huang '910 uses the BIST test to determine bad memory locations from a memory block and then "associates" or "pairs" a good memory location in a redundant memory with the determined bad memory location from the memory block via a repair table. Once the association between the bad memory and the good redundant memory is finished, then the BIST re-tests the memory, and skips the bad memory locations during the test and instead tests the associated redundant memory locations in their place, as specified in the repair table. However, nowhere in the testing process described in Huang '910 is there any teaching or discussion of repeating selection of **an alternate** redundant memory section, if the selected redundant memory section or the selected alternate redundant memory section is non-functional, until at least one of the selected redundant memory section or the selected alternated redundant memory section is determined to be functional or all redundant memory sections have been selected.

In the "Response to Arguments" section, the Office Action alleged that "repeating selection of **an alternate** redundant memory section, if the selected redundant memory section or the selected alternate redundant memory section is non-functional, until at least one of the selected redundant memory section or the selected alternated redundant memory section is determined to be functional or all redundant memory sections have been selected" is equivalent to testing of the memory and the redundant memory locations. In the present invention, first, the memory section is tested to see if it is functional. If the memory section is not functional, a redundant memory section is selected and a determination is made as to whether the redundant memory section is functional. If the redundant memory section is also not functional, an alternate redundant memory section is selected is tested to see if the alternate redundant memory section is functional. The step of selecting the alternate redundant memory section is repeated until the selected memory section is determined to be functional or all redundant memory sections have been selected.

As noted above, in Huang '910 the selected redundant memory is the memory that is subject to testing such that the faulty rows are failed over to good redundant rows. Col. 9, lines 5-15 of

Huang '910 discloses that when the BIST retests the first m rows of memory, it is actually testing a combination of accessible and redundant rows that tested good in the first stage and if an error occurs in the first m rows during the second stage, the memory is considered non-repairable. Also see Col. 9, line 52 – Col. 10, line 9 of Huang '910. Thus, in Huang '910, no subsequent selection and testing is done.

Thus, Applicant submits that Huang '910 discloses that the testing process is only being performed twice. So, according to Huang, one BIST test is conducted to determine bad memory locations, and then after the repair table and associations are created, a second BIST test is conducted to make sure that the associations function properly. If the second BIST test fails, the method of Huang '910, as disclosed in Col. 8, lines 40-45 and Col. 9, line 52 – Col. 10, line 9, quits and determines that the memory is faulty and not useable. On the other hand, according to the present invention as disclosed in paragraph 0024-0029 of applicant's specification and recited in the presently pending claims, after the failed memory is replaced by a redundant memory, a second test is performed to check the redundant memory. If the redundant memory is also faulty, alternative redundant memory sections may be selected until the SRAM is determined to be functional or until all redundant memory sections have been tested. Therefore, after selection of alternative redundant memory sections, further tests are performed to determine if those memory sections are acceptable. In order to track which memory sections are currently redundant, the present invention, as recited in the present pending claims, updates the redundant memory data structure to indicate that a selected redundant memory section or selected alternate redundant memory section is no longer redundant.

Contrary to the present invention, there is no disclosure nor support for the testing method of Huang '910 updating a redundant memory structure to indicate that a block of the redundant memory (the block used to cover for the bad memory block location) is no longer available, as there is no third or additional testing and association step in Huang '910 that would require further association of an available redundant memory location with a bad memory location. Given the disclosure of Huang '910, Applicants respectfully assert that the rejection under 35 U.S.C. §102(e) is erroneous and should be withdrawn because Huang '910 does not teach or suggest each feature of claims 1, 10 and 11. Applicant submits that because claims 2-6 and 14-16 depend from claims 1, 10 and 11, claims 2-6 and 14-16 are allowable at least for the same reasons as claims 1, 10 and 11 as well as for the additional features recited in claims 2-6 and 14-16.

Claim 12 was rejected under 35 U.S.C. §103(a) as being unpatentable over Huang '910 in view of U.S. Publication No. 20020136066 to Huang (hereinafter Huang '066). The Office Action took the position that Huang '910 teaches each and every element recited in claim 12, except for the

self adaptive logic limitations. Therefore, the Office Action combined Huang '910 and Huang '066 in an effort to yield all of the elements of claim 12. As outlined below, Huang '910 and Huang '066 fail to disclose or suggest each of elements of claim 12. The failure of Huang '910 and Huang '066 to disclose each and every element of the present claims constitutes clear error, and withdrawal of this rejection is required.

Claim 13 was rejected under 35 U.S.C. §103(a) as being unpatentable over Huang '910 in view of U.S. Patent No. 6,993,696 to Tanizaki (hereinafter Tanizaki). The Office Action took the position that Huang '910 teaches each and every element recited in claim 13, except for the state of a pin. However, the Office Action combined Huang '910 with Tanizaki in an effort to yield all of the elements of claim 13. As outlined below, Huang '910 and Tanizaki fail to disclose or suggest each of elements of claim 13. The failure of Huang '910 and Tanizaki to disclose each and every element of the present claims constitutes clear error, as outlined below.

Claims 8 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Huang '910 in view of U.S. Patent No. 6,181,614 to Aipperspach (hereinafter Aipperspach). The Office Action took the position that Huang '910 teaches each and every element recited in claims 8 and 18, except for where the method of performed during the manufacturing process. However, the Office Action combined Huang and Aipperspach in an effort to yield all of the elements of claims 8 and 18. As outlined below, Huang '910 and Aipperspach fail to disclose or suggest each of elements of claims 8 and 18. The failure of Huang '910 and Aipperspach to disclose each and every element of the present claims constitutes clear error, as outlined below.

Claims 9 and 19 stand rejected under 35 U.S.C. §103(a) as being obvious over Huang '910 in view of U.S. Publication No. 20030014619 to Cheston (hereinafter Cheston). The Office Action took the position that Huang'910 teaches each and every element recited in claims 8 and 18, except for where the method is performed during circuit power up. However, the Office Action combined Huang '910 with Cheston in an effort to yield all of the elements of claims 9 and 19. As outlined below, Huang '910 and Cheston fail to disclose or suggest each of elements of claims 9 and 19. The failure of Huang '910 and Cheston to disclose each and every element of the present claims constitutes clear error, as outlined below.

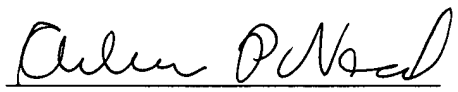
Neither Huang '066, Tanizaki, Aipperspach nor Cheston cures any of the deficiencies of Huang '910, as noted above. Specifically, none of these secondary references teaches or suggests a BIST that is capable of repeating selection of an alternate redundant memory section, if the selected redundant memory section or the selected alternated redundant memory section is non-functional, until at least one of the selected redundant memory section or the selected alternated redundant

memory section is determined to be functional or all redundant memory sections have been selected, as recited in claims 1 and 11, upon which claims 8, 9, 12, 13, 18 and 19 depends. Therefore, Applicant asserts that the rejections under 35 U.S.C. 103(a) are erroneous and should be withdrawn because neither Huang '910 and Huang '066, Tanizaki, Aipperspach nor Cheston, whether taken singly or combined, teaches or suggests the combination of elements recited in claims 1 and 11. Applicant submits that because claims 8, 9, 12, 13, 18 and 19 depend from claims 1 and 11, claims 8, 9, 12, 13, 18 and 19 are allowable at least for the same reasons as claims 1 and 11 as well as for the additional features recited in claims 8, 9, 12, 13, 18 and 19.

For all of the above noted reasons, it is strongly submitted that certain clear differences exist between the present invention as claimed in claims 1-6, 8-16, 18 and 19 and the prior art relied upon by the Examiner. It is further submitted that these differences are more than sufficient that the present invention would not have been anticipated or obvious to a person having ordinary skill in the art at the time the invention was made. This final rejection being in clear error, therefore, it is respectfully requested that the Examiner's decision be reversed in this case regarding the rejections of claims 1-6, 8-16, 18 and 19, and indicate the allowability of all of pending claims 1-6, 8-16, 18 and 19.

Reconsideration and withdrawal of the rejections, in view of the clear errors in the Office Action, is respectfully requested. In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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Enclosures: PTO/SB/33 Form
Notice of Appeal
Petition for Extension of Time
Check No. 17949